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| 09/941,557 | 08/30/2001 | R. J. Baker | M4065.0474/P474 | 6108 |

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DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street, NW
Washington, DC 20037

| EXAMINER | |
|---|---|
| TRAN, DZUNG D | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2613 | |

DATE MAILED: 06/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/941,557 | BAKER ET AL. | |
| | Examiner | Art Unit | |
| | Dzung D. Tran | 2613 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9, 12, 14-36, 38-53, 56, 58-89, 91, 92, 94, 97, 98, 100-108, 111-113, 115-133, and 136-162* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 1-9,12,14-36,38-53,56,58-89,91,92,94,97,98,100-108,111-113,115-133 and 136-162.

## DETAILED ACTION

### *Specification*

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 89, 92, 101 and 126 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vogley European patent no. EP 0849685 in view of Yasuda US patent no. 6,529,534.

Regarding claim 1, Vogley discloses in figure 1 a communication bus system between processors and memory modules comprising:

a memory controller 12 (col. 2, line 25);

at least one memory storage device 20 (col. 2, lines 26-27); and

a continuous optical path 16, 22 (col. 3, line 19, col. 4, lines 1-4) coupled to said memory controller 12 and to memory bus (e.g., elements 18, 22) arranged and configured for exchanging data between said memory controller and said at least one memory storage device 20, said optical path 16 comprising an electro-optical converter 14 arranged and configured to convert an electrical signal output from said controller to an optical signal for transmission on said continuous optical path 16. Vogley differs

from claim 1 of the present invention in that he does not specifically disclose the optical transmitter 14 is a wavelength adjustable optical transmitter. Yasuda discloses a well known wavelength adjustable optical transmitter (see Figure 3) having a wavelength controlling circuit for adjusting the output wavelength of the laser (abstract, col. 1, lines 8-12, col. 4, line 52 to col. 5, line 38). At the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to replace the well known wavelength adjustable optical transmitter taught by Yasuda with the optical transmitter 14 in the system of Vogley. One of ordinary skill in the art would have been motivated to do in order to set a laser signal to a target wavelength readily upon wavelength control of the laser signal and eliminates the problem of drift (col. 2, lines 3-7 of Yasuda).

Regarding claim 2, Vogley discloses memory controller 12 transmits data to said at least one memory storage device through said optical path 16, 22 (e.g., the memory controller is operable to transmit data to the memory device via the optical fiber 16 and the memory modules are operable to transmit data to the memory controller 12 via communication bus is formed from optical fiber; col. 3, lines 19-21, col. 4, lines 1-4).

Regarding claim 3, Vogley discloses memory controller and said at least one data includes at least one of memory device 20 are arranged and configured to exchange read/write data (e.g, since the controller is a processor (i.e., it is inherently that controller can be configured to read/write data) and since the memory is a DRAM, SRAM; see col. 2, lines 21-22, it is inherently that memory can be configured to read/write data).

Regarding claim 4, Vogley discloses the continuous optical path 16 includes at least one optical link 18 for exchange read/write data.

Regarding claim 5, Vogley discloses data includes address data transmitted from said memory controller 12 to said at least one memory storage device 20 (col. 2, lines 38-39).

Regarding claims 89, 92, 101 and 126, Yasuda disclose the optical transmitter 3 (same as an electro-optical converter) comprising:

at least one input 32, 33 arranged and configured to receive an electrical data signal from a memory controller;

at least one optical output arranged and configured to transmit said optical signal into optical path.

3. Claims 6-8, 12, 14, 24-36, 38-41, 44-51, 53, 56, 58, 68-71, 73-85, 88, 91, 94-95, 97, 98, 100, 102-107, 115-123, 127-132, 139-148, 150-151, 155 and 159 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vogley European patent no. EP 0849685 in view of Yasuda US patent no. 6,529,534 and further in view of Acton et al. US patent no. 5,544,319.

Regarding claims 6, 105 and 130, as per claims above, Vogley and Yasuda discloses all the limitations except for data includes command data transmitted from said controller to said at least one memory storage device. Acton, from the same field of endeavor, discloses data includes command data transmitted from said controller to said at least one memory storage device (col. 16, lines 20-22).

. At the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to include the teaching of Acton in the system of Vogley and Yasuda. One of ordinary skill in the art would have been motivated to do in order to control the information between the memory controller and the memory storage device.

Regarding claim 7, Acton discloses optical path 4 includes an optical link for transmission a clock signal (col. 9, lines 50- 51).

Regarding claim 8, Acton discloses optical path 4 includes an optical link for transmission control data (figure 4, col. 6, line 24).

Regarding claims 102 and 127, Acton discloses controller receives data from said at least one memory storage device through said optical path 4 (col. 2, lines 48-60).

Regarding claims 103 and 128, Acton discloses data includes at least one of read and write data (abstract, col. 2, lines 48-51).

Regarding claims 104 and 129, Acton discloses data includes address data transmitted from said controller to said at least one memory device (figure 3, col. 3, line 49, col. 5, lines 54-62).

Regarding claims 106 and 131, Acton discloses data includes a clock signal (col. 9, lines 50- 51).

Regarding claims 107 and 132, Acton discloses data includes control data (figure 4, col. 6, line 24).

Regarding claims 12 and 14, Acton discloses receiver 19 (same as an electro-optical converter) for converting an optical signal on said optical path 4 to an electrical

signal and transmitting said electrical signal to said controller 1 and memory storage device (col. 2, lines 44-48).

Regarding claims 24, 68 and 139, Acton discloses at least one memory device is located memory coupled system (e.g. same as a memory module) (col. 2, lines 44-48).

Regarding claims 25, 69, 115 and 140, Acton discloses the bus 5 of each memory coupled system is connected to an optical fiber 4 to memory coupling system controller (col. 2, lines 48-50).

Regarding claims 26-28, 70-72 and 116-117, Yasuda discloses in Figure 3, wavelength sensing mechanism (e.g., wavelength monitoring circuit 4) connect to controller 1 arranged and configured to provide wavelength information to said controller 1 and wherein said wavelength sensing mechanism (e.g., wavelength monitoring circuit 4) is located at a controller side and controller 1 is arranged to provide wavelength adjustment to said LD 3.

Regarding claim 44, Acton discloses memory module comprises an electro-optical converter 19 of figure 2 for connecting optical data from said optical path 4 to electrical signals for said at least one memory device from the node 6 (col. 2, lines 44-48).

Regarding claims 29, 73 and 76, Acton discloses in figure 1, a single optical path 4 between said controller 1 and at least one memory device 5 for exchanging at least read/write data (abstract, col. 2, lines 48-51) present on a plurality of electrical paths (figure 3) between said controller 1 and at least one memory storage device 5 (col. 3, lines 31-47).

Regarding claim 30, 34, 74, 78, 119 and 144, Acton discloses single optical path 4 further arranged and configured to exchange data includes command data transmitted from said controller to said at least one memory device (col. 16, lines 20-22).

Regarding claims 31, 35, 75, 79, 120 and 145, Acton discloses single optical path 4 further arranged and configured to exchange data includes address data transmitted from said controller to said at least one memory device (figure 3, col. 3, line 49, col. 5, lines 54-62).

Regarding claims 32, 36, 80 and 81, Acton discloses single optical path 4 further arranged and configured to exchange data includes a clock signal (col. 9, lines 50- 51).

Regarding claims 33, 77, 118 and 143, Acton discloses in figures 2 and 3, data includes read/write data which originates on a plurality of electrical paths, said optical path 4 comprising a plurality of discrete optical guides respectively associated with said electrical path (col. 3, lines 22-30).

Regarding claims 38 and 82, Acton discloses data includes control data (figure 4, col. 6, line 24).

Regarding claims 39, 83, 121 and 146, Acton discloses in figure 1, controller 1, at least one memory device 5, and optical path 4 are all integrated on the same die.

Regarding claims 40, 84, 122 and 147, Acton discloses in figure 1, a processor (col. 2, line 47) for communicating with said at least one memory device, wherein said controller 1, at least one memory device, processor, and optical path are all integrated on the same die (figure 1).

Regarding claims 41, 123 and 148, Acton discloses a processor (col. 2, line 47) for communicating with said at least one memory device from the node 6 (col. 2, lines 44-48), wherein said, processor and said at least one memory device are provided on separate dies and communicate via said optical path 4.

Regarding claim 45, Acton discloses a processor (col. 2, line 47);

Regarding claims 46 and 47, Acton discloses controller 1 for exchange data to and from said at least one memory storage device from the node 6 (col. 2, lines 44-48) through said optical path 4 (see figure 1).

Regarding claim 48, Acton discloses optical path 4 includes at least one optical link for exchange of read and write data (abstract, col. 2, lines 48-51).

Regarding claim 49, Acton discloses optical path 4 includes an optical link for address data transmitted from said controller to said at least one memory storage device (figure 3, col. 3, line 49, col. 5, lines 54-62).

Regarding claim 50, Acton discloses optical path 4 includes an optical link for command data transmitted from said controller to said at least one memory storage device (col. 16, lines 20-22).

Regarding claim 51, Acton discloses optical path 4 includes an optical link for transmission a clock signal (col. 9, lines 50- 51).

Regarding claim 52, Acton discloses optical path 4 includes an optical link for transmission control data (figure 4, col. 6, line 24).

Regarding claims 56, 58 and 88, Acton discloses optical receiver 19 (same as an electro-optical converter) for converting an optical signal on said optical path 4 to an

electrical signal and transmitting said electrical signal to said controller 1 (col. 2, lines 44-48).

Regarding claims 91 and 94, Yasuda discloses transmitter 3 include laser optical source (see Figure 3).

Regarding claims 95 and 98, Acton discloses optical receiver 19 (same as an electro-optical converter) at least one input (input from fiber 4) for receiving a optical data signal from an optical path 4; at least one electro-optical converter (e.g. receiver 19) for converting said received data signal to an electrical signal and at least one electrical output (output to LATCH 15, 17) for transmitting said output signal to an electrical path of a memory controller 1 or memory device from the node 6 (col. 2, lines 44-48).

Regarding claims 97 and 100, Yasuda discloses an optical receiver 43, 44 includes a photodiode (see Figure 3).

Regarding claims 39, 83, 84, 121, 122, 146 and 147, Acton discloses processor (col. 2, line 47), controller 1, at least one memory device (col. 16, lines 20-22) and optical path 4 are all integrated on the same die (see figure 1).

Regarding claims 41, 85, 123 and 148, Acton discloses processor (col. 2, line 47) and at least one memory device (col. 16, lines 20-22) are provided on separate dies and communicate via said optical path 4 (see figure 1).

Regarding claims 151, 155 and 159, multiplexed optical channels use TDM is well known in the art (for example SONET system).

5. Claims 9, 15-23, 42, 43, 52, 59-67, 86, 87, 108, 111-113, 124, 125, 133, 136-138, 149, 152-154, 156-158 and 160-162 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vogley European patent no. EP 0849685 in view of Yasuda US patent no. 6,529,534 and Acton et al. US patent no. 5,544,319.

further in view of Fee US Patent no. 6,658,210.

Regarding claims 9, 52, 108 and 133, as per claims above, the combination of Vogley, Yasuda and Acton discloses all the limitations except for optical path comprises a plurality of multiplexed optical channels, said data being transmitted over said multiplexed optical channels. Fee discloses a WDM optical system comprising a bi-directional optical fiber has a plurality wavelengths to carry information (abstract) and data being transmitted over multiplexed optical channels (e.g. WDM, see col. 2, lines 47-55). At the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to incorporated WDM coupler for multiplexing and de-multiplexing optical signals of Fee in the combination of Vogley, Yasuda and Acton. One of ordinary skill in the art would have been motivated to do this since Wavelength Division Multiplexing Multiplex/Demultiplex coupler offers advantages of allowing the optical signals transmits back and forth over an bi-directional optical link and allow multi-wavelengths to communicate via single fiber or wave guide.

Regarding claims 15, 59, 111, 112, 136 and 137, the combination of Vogley, Yasuda, Acton and Fee discloses a multiplexer/demultiplexe (220 of figure 3 of Fee) associated with said controller (1 of figure 1 of Acton) for multiplexing said optical

channels, and associated with said at least one memory device (5 of figure 1 of Acton) for demultiplexing said multiplexed optical channels.

Regarding claims 16 and 60, the combination of Vogley, Yasuda, Acton and Fee discloses a multiplexer/demultiplexe (226 of figure 3 of Fee) associated with said at least one memory device (5 of figure 1 of Acton) for multiplexing optical channels and providing multiplexed optical channels to said optical path 4 and associated with said memory controller (1 of figure 1 of Acton) for demultiplexing said multiplexed optical channels.

Regarding claims 17, 61, 113 and 138, the combination of Vogley, Yasuda, Acton and Fee discloses a multiplexer/demultiplexe (220, 226 of figure 3 of Fee) located on each side of said optical path.

Regarding claims 18 and 62, Acton discloses data includes at least one of read and write data (abstract, col. 2, lines 48-51).

Regarding claims 19 and 63, Acton discloses data includes command data transmitted from said controller to said at least one memory device (col. 16, lines 20-22).

Regarding claims 20 and 64, Acton discloses data includes address data transmitted from said controller to said at least one memory device (figure 3, col. 3, line 49, col. 5, lines 54-62).

Regarding claims 21 and 65, Acton discloses data includes a clock signal (col. 9, lines 50- 51).

Regarding claims 22 and 66, Acton discloses data includes control data (figure 4, col. 6, line 24).

Regarding claims 23 and 67, Acton discloses electrical paths connected between said controller 1 and said at least one memory device 5 for passing data between said controller and memory device (see figure 3).

Regarding claims 152-155, 156-157, 160 and 161, Fee discloses multiplexed optical channels use WDM (see col. 2, lines 47-55).

Regarding claims 42, 43, 86, 87, 124, 125, 149 and 150, Acton discloses processor (col. 2, line 47) and at least one memory device (col. 16, lines 20-22) are provided on separate dies and communicate via said optical path 4 (see figure 1). However, having the separate dies in a common package or separated package is merely an engineering design choice.

Regarding claims 154, 158 and 162, transmitting compressed data is well known in the art.

## *Response to Arguments*

4. Applicant's arguments with respect to claims 1-9, 12, 14-36, 38-53, 56, 58-89, 91, 92, 94, 97, 98, 100-108, 111-113, 115-133, and 136-162 have been considered but are moot in view of the new ground(s) of rejection.

## *Conclusion*

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dzung Tran whose telephone number is (571) 272-3025.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, Jason Chan, can be reached on (571) 272-3022.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Dzung Tran

Dzung Tran

06/09/2006